IN THE SPECIFICATION:

Please replace the paragraph beginning on Page 10, line 21, with the following amended paragraph:

Within each receiver logic block, OR gates 214 receive the outputs of multiplexers 920. Each multiplexer 920 may be configured to select for a non-cascaded input. With respect to macrocell 0, multiplexers 920 would thus select for product term outputs 1120 A0_0 through A0_4. However, to achieve wider input logic functions, multiplexers 920 may be configured to select for outputs 910 of AND gates 900. AND gates 900 correspond to the product terms 1120 on a one-to-one basis. For example, with respect to macrocell 0, there is one AND gate 900 for each of product term outputs A0_0 through A0_4. When fuse points 905 are activated each AND gate 900 receives its product term (one of product terms A0_0 through A0_4) and the corresponding one from the feeder logic block (one of product terms B0_0 through B0_4). For ease of design and programmability, fuse points 905 for one macrocell may be all under the control of just one configuration memory cell. Thus, in such an embodiment, the product term cascading occurs solely at a macrocell level – the product terms for a single macrocell may not be selectively cascaded with respect to each other. However, in alternate embodiments, each fuse point 905 may be under the control of its own configuration memory cell. In this case, for example, just product terms A0_0 and B0_0 may be cascaded. Referring back to Figure 3, a receiver logic block such as programmable logic block 302B may act as a feeder logic block for another receiver logic block such as 302C within a cascade chain. For a receiver logic block acting also as a feeder logic block, outputs 910 from AND gates 900 travel on dedicated paths analogously to paths 920 to AND gates 900 within the next receiver logic block in the cascade chain. Within a

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cascade chain, only the very first logic block and last logic block (such as programmable logic blocks 302H and 302E) do not have a dual role as both a feeder and a receiver logic block. In a feeder logic block, macrocell 104 may be configured to not register its own product terms if these product terms are being cascaded. In such a case, macrocell 104 can be used (1) for logic functions and borrow product terms from other macrocells through the PTSA 204 (Figure ~~3~~ 4) or (2) as an input register coupled to an I/O pad 242 (Figure 3).

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